IN THE CLAIMS:

Claims 9 and 23 – 26 have been amended. Claims 27 - 29 have been added.

1. (previously presented) An input protection circuit comprising:

an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

a second well region of the first conductivity type formed in the principal surface area of said semiconductor substrate;

third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base, bottoms of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate; and a circuit formed in said semiconductor substrate and connected to said input terminal;

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region, said first lateral bipolar transistor operating without a fixed base bias, and said fourth well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

2. (original) An input protection circuit according to claim 1, further comprising a current limiting resistor formed on an insulating layer formed in the principal surface area of said semiconductor substrate, wherein said input terminal is connected via said current limiting resistor to said first impurity doped region.

Claims 3 and 4 (cancelled).

5. (original) An input protection circuit comprising:

an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

second and third well regions of a second conductivity type formed in the principal surface area of said semiconductor substrate, said second and third well regions forming a second lateral bipolar transistor with a portion of said semiconductor substrate serving as a base;

a circuit formed in said semiconductor substrate and connected to said input terminal;

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region, said first lateral bipolar transistor operating without a

fixed base bias, and said third well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

6. (original) An input protection circuit according to claim 5, further comprising a current limiting resistor formed on an insulating layer formed in the principal surface area of said semiconductor substrate, wherein said input terminal is connected via said current limiting resistor to said first impurity doped region.

Claims 7 -8 (previously cancelled).

9. (currently amended) A semiconductor input protection circuit comprising:

a semiconductor substrate;

a first active region of a first conductivity type defined in said semiconductor substrate;

a second active region of a second conductivity type defined in said semiconductor substrate;

first and second impurity doped regions of the second conductivity type formed in said first active region;

third and fourth impurity doped regions of the first conductivity type formed in said second active region;

an input terminal connected to said first impurity doped region;

a first wiring for connecting said first active region and said second impurity doped region to said third impurity doped region; and

a second wiring for connecting only said second active region and said fourth impurity doped region to a reference potential.

10. (original) A semiconductor input protection circuit according to claim 9, wherein said semiconductor substrate is of the second conductivity type and said third and fourth impurity doped regions reach a bottom of said second active region.

Claim 11 (cancelled).

12. (original) A semiconductor input protection circuit according to claim 10, wherein said second active region is a portion of said semiconductor substrate.

Claim 13 (cancelled).

14. (original) A semiconductor input protection circuit according to claim 9, further comprising:

an insulating film formed on said semiconductor substrate; and

a polysilicon resistor formed on said insulating film,

wherein said input terminal is connected via said polysilicon resistor to said firs impurity doped region.

15. (original) A semiconductor input protection circuit according to claim 9, further comprising:

a first contact region of the first conductivity type having a high impurity concentration, and formed in said first active region outside said first and second impurity doped regions, wherein said first wiring is connected via said first contact region to said first active region.

16. (original) A semiconductor input protection circuit according to claim 15, wherein said first contact region and said third and fourth impurity doped regions have substantially the same impurity concentration and depth.

17. (original) A semiconductor input protection circuit according to claim 9,

further comprising:

a second contact region of the second conductivity type having a high impurity concentration, and formed in said second active region outside said third and fourth impurity doped regions, wherein said second wiring is connected via said second contact region to said second active region.

18. (original) A semiconductor input protection circuit according to claim 15, wherein said second contact region and said first and second impurity doped regions have substantially the same impurity concentration and depth.

19. (original) A semiconductor input protection circuit according to claim 10, further comprising:

a first contact region of the first conductivity type having a high impurity concentration, and formed in said first active region outside said first and second impurity doped regions, wherein said third and fourth impurity doped regions each include a surface side high impurity concentration region and a deeper low impurity concentration region, and have substantially the same impurity concentration and depth as said surface side high impurity concentration region and said first contact region.

Claims 20 – 22 (cancelled).

23. (currently amended) The input protection circuit of claim 1, wherein the second lateral bipolar transistor is turned on to protect the input protection circuit when a high positive bias voltage ~~of a first polarity, the first polarity corresponding to the first conductivity type,~~ is applied to the input terminal.

24. (currently amended) The input protection circuit of claim 1, wherein the first lateral bipolar transistor is turned on to protect the input protection circuit when a high

negative bias voltage ~~of a second polarity, the second polarity corresponding to the second conductivity type,~~ is applied to the input terminal.

25. (currently amended) The input protection circuit of claim 5, wherein the second lateral bipolar transistor is turned on to protect the input protection circuit when a high positive bias voltage ~~of a first polarity, the first polarity corresponding to the first conductivity type,~~ is applied to the input terminal.

26. (currently amended) The input protection circuit of claim 5, wherein the first lateral bipolar transistor is turned on to protect the input protection circuit when a high negative bias voltage ~~of a second polarity, the second polarity corresponding to the second conductivity type,~~ is applied to the input terminal.

27. (new) The input protection circuit of claim 1, wherein the third well region is formed entirely inside the second well region.

28. (new) The input protection circuit of claim 1, wherein the third and fourth well regions have a depth almost equal to the second well region.

29. (new) The input protection circuit of claim 1, wherein the third and fourth well regions are not part of a MOS transistor.